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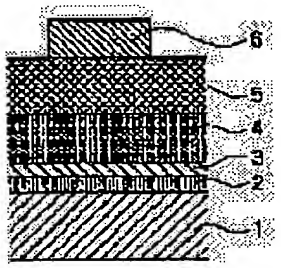
(54) FERROELECTRIC THIN FILM ELEMENT, FABRICATION THEREOF, AND FERROELECTRIC MEMORY ELEMENT

(57)Abstract:

PROBLEM TO BE SOLVED: To crystallize a ferroelectric thin film by coating a substrate with a precursor solution containing the constitutive elements of ferroelectric thin film material, drying the solution to form a thin film, subjecting the thin film to heat treatment to form a ferroelectric thin film, and then heating ferroelectric thin film in an atmosphere of specified gas pressure.

SOLUTION: A film is formed using a precursor solution containing Ta, Bi and Sr. More specifically, a substrate having a lower platinum electrode 4 is spin coated with a precursor solution. The substrate is then mounted on a heated hot plate and baked in the atmosphere. The filming step is repeated to form a ferroelectric thin film 5. Subsequently, heat treatment is performed, as first baking, in an oxygen atmosphere of atmospheric pressure by RTA and a Pt upper electrode 6 is deposited using a mask by EB deposition. After forming the upper electrode, second baking is



performed by RTA method in an oxygen atmosphere of 10Torr which is lower than 1atm. Second baki.nq is performed in order to crystallize the ferroelectric thin film perfectly.

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CLAIMS

[Claim(s)]

[Claim 1] In the manufacture approach of the ferroelectric thin film equipped with a lower electrode layer, a ferroelectric thin film, and an up electrode layer in order on a substrate The process which applies the precursor solution containing a metal to the front face of said lower electrode layer formed on the substrate, The process which heats the applied precursor solution, removes only a solvent and is dried, The manufacture approach of the ferroelectric thin film characterized by including the 1st heat treatment process which heats the dried precursor and forms a ferroelectric thin film, and the 2nd heat treatment process heated in a gas pressure ambient atmosphere lower than one atmospheric pressure after forming an up electrode layer on this ferroelectric thin film.

[Claim 2] The manufacture approach of a ferroelectric thin film according to claim 1 that gas pressure of the ambient atmosphere of said 2nd heat treatment process is characterized by being 20 or less Torrs.

[Claim 3] The manufacture approach of a ferroelectric thin film according to claim 2 that gas pressure of the ambient atmosphere of said 2nd heat treatment process is characterized by 2 or more Torrs being 20 or less Torr.

[Claim 4] The manufacture approach of a ferroelectric thin film given in any 1 term of claims 1–3 to which heating temperature of said 2nd heat treatment process is characterized by 500–degree–C or more being 650 degrees C or less.

[Claim 5] The manufacture approach of a ferroelectric thin film given in any 1 term of claims 1–4 to which said precursor solution is characterized by using metaled carboxylate and a metaled alkoxide as a component.

[Claim 6] The ferroelectric thin film to which said ferroelectric thin film is characterized by the diameter of the maximum crystal grain consisting of a bismuth layer structure compound 700A or less in the ferroelectric thin film equipped with the lower electrode layer, the ferroelectric thin film, and the up electrode layer in order on the substrate.

[Claim 7] In the semiconductor memory component containing the memory cell equipped with one transistor for a switch, and one ferroelectric capacitor The semi–conductor substrate top with which said transistor for a switch was formed The insulator thin film of a wrap 1st, this — with the contact plug into which it pierced through the 1st insulator thin film, and the interior was filled up with conductive material The ferroelectric memory device characterized by having the stack mold structure equipped with the lower electrode formed on this contact plug, the ferroelectric thin film formed on this lower electrode, and the up electrode formed on this ferroelectric thin film, and said ferroelectric thin film consisting of a bismuth layer structure compound.

[Claim 8] The ferroelectric memory device according to claim 7 to which the bismuth layer structure compound which accomplishes said ferroelectric thin film is characterized by being the compound of Ta or Ti which contains either at least including Sr and Bi.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention] This invention relates to the manufacture approach of the ferroelectric thin film used for a memory device, a pyroelectric sensor component, a piezoelectric device, etc., a ferroelectric thin film, and a ferroelectric memory device.

[0002]

[Description of the Prior Art] Since a ferroelectric thin film has many functions, such as spontaneous polarization, a high dielectric constant, the electro-optical effect, the piezo-electric effect, and a pyroelectric effect, it is applied to extensive device development. for example, the pyroelectricity — using — an infrared linear array sensor — moreover, piezoelectric [the] — using — an ultrasonic sensor — the electro-optical effect — using — an optical waveguide modulator — the high dielectric — using — DRAM and the capacitor for MMIC — ** — it is used in various directions.

[0003] Also in those extensive application device development, development of the ferroelectric nonvolatile memory (FRAM) which is high-density and operates at a high speed with combination with a semiconductor memory technique with progress of thin film coating technology in recent years is prosperous. The researches and developments by which it reads and the nonvolatile memory using a ferroelectric thin film turns to utilization as memory in which the high-speed writing / not only replacement of the nonvolatile memory of the former [properties /, such as height of low-battery actuation and writing / read-out resistance,] but the replacement to SRAM or DRAM is also possible are done briskly.

[0004] A coercive field (Ec) is small, a remanence (Pr) is large and an ingredient with the big repeat resistance of polarization reversal is [it is low leakage current and] required for such device development. Furthermore, since reduction of operating voltage and a semi-conductor micro-processing process are suited, it is desirable to realize the above-mentioned property with the thin film of 200nm or less of thickness.

[0005] And as a ferroelectric ingredient used for these applications, the oxide ingredient of the perovskite structure represented by PZT (titanic-acid lead zirconate, Pb(Ti, Zr) O3) was in use. However, since the ingredient which contains lead as the configuration element like PZT has the high vapor pressure of lead or its oxide, lead evaporates at the time of membrane formation, a defect is generated in the film, or when severe, it forms a pinhole. Consequently, when leakage current increased or polarization reversal was repeated further, there was a fault, like the fatigue phenomena to which the magnitude of spontaneous polarization decreases happen. If the replacement to FRAM by ferroelectric nonvolatile memory is considered especially, in order to have to guarantee that after 1015 polarization reversal does not have change of a property about fatigue phenomena, development of a ferroelectric thin film without fatigue was desired.

[0006] On the other hand, researches and developments of a bismuth layer structure compound ingredient are done in recent years. The bismuth layer structure compound ingredient was discovered by Smolenskii and others in 1959 (G. A.Smolenskii, V.A.Isupov and A.I.Agranovskaya, Soviet Phys.Solid State, 1,149 (1959)), and a detailed examination was made by Subbarao after that (E. C.Subbarao,

J.Phys.Chem.Solids, 23,665 (1962)). Recently, Carlos A.Paz de Araujo and others discovers that this bismuth layer structure compound thin film fits the application to a ferroelectric and a high dielectric integrated circuit, and after 1012 polarization reversal or more has reported especially the outstanding fatigue property that change is not looked at by the property (International Application No.PCT/US 92/10542).

[0007] moreover, the sol gel process or MOD (Metal OrganicDecomposition) which uses physical methods, such as vacuum evaporation technique, the sputtering method, and the laser ablation method, and an organometallic compound as a start raw material at the manufacture approach of a ferroelectric thin film, carries out pyrolysis oxidation of these, and obtains an oxide ferroelectric — law and MOCVD (Metal Organic Chemical Vapor Deposition) — the chemical approaches, such as law, are used.

[0008] special vacuum devices are unnecessary and membrane formation of a large area is [that homogeneous mixing of atomic level is possible for a sol gel process or the MOD method in the above-mentioned forming-membranes method, presentation control being easy and excelling in repeatability, and] possible at ordinary pressure — it is low cost industrially — etc. — it is widely used from the advantage.

[0009] Especially as the membrane formation approach of the above-mentioned bismuth layer structure compound thin film, the MOD method is used and a ferroelectric thin film or a dielectric thin film is manufactured at the following processes by the membrane formation process of the conventional MOD method (International Application No.PCT/US 92/10542, PCT/US 93/10021).

[0010] 1) The process which carries out spreading membrane formation of the precursor solution which consists of compound ARUKISHIDO etc. on a substrate with a spin coat method etc.

[0011] 2) The process which carries out stoving of the obtained film for 30 seconds to several minutes at 150 degrees C in order to make it secede from alcohol and the residual moisture which carried out reaction generation in the solvent or the process of 1 from the inside of the film.

[0012] 3) in order to carry out pyrolysis removal of the organic substance component in the film — RTA (Rapid Thermal Annealing) — the process heat-treated for 30 seconds at 725 degrees C in an oxygen ambient atmosphere using law.

[0013] 4) The process heat-treated at 800 degrees C in an oxygen ambient atmosphere for 1 hour in order to crystallize the film.

[0014] 5) The process heat-treated for 30 minutes at 800 degrees C in an oxygen ambient atmosphere after forming an up electrode.

[0015] In addition, in order to obtain desired thickness, the process of 1-3 is repeated and, finally 4 or 5 processes are performed.

[0016] A ferroelectric thin film or a dielectric thin film can be manufactured as mentioned above.

[0017]

[Problem(s) to be Solved by the Invention] However, in the manufacture approach of the ferroelectric thin film by the above conventional MOD methods, with the burning temperature of 650 degrees C or less, the ferroelectric thin film by the process (process 4) which crystallizes before forming an up electrode needed to carry out thing long duration heat-treatment at the elevated temperature extremely with 800 degrees C for 1 hour, in order to hardly crystallize but to acquire a high remanence value (International Application No.PCT/US 93/10021). For this reason, since dielectric strength also fell and micro processing became difficult further while particle diameter became ****** of the magnitude which is about 2000A and leakage current increased, it was not suitable for high integration.

[0018] Moreover, in the conventional MOD method, since there was a problem of a crack occurring when thickness obtained on 1 time of a spin coat is made into about 1000A or more, the concentration of a precursor solution was adjusted so that it might become 1000A or less about the thickness obtained on 1 time of a spin coat. Therefore, in order to obtain about 2000A thickness, whenever several times of spreading processes were needed and it applied once by the spin coater, heat treatment by RTA was needed, and it was very unproductive on the manufacture process of a component.

[0019] On the other hand, in order to integrate ferroelectric nonvolatile memory highly, it is necessary

to connect a ferroelectric capacitor with a selection transistor with a contact plug, and to adopt the stack mold structure in which the ferroelectric capacitor was formed on the contact plug (S. Onishi et al., IEEE IEDM Technical Digest, p.843 (1994)). However, heat-treatment of long duration has problems, such as causing the poor contact and property degradation by the counter diffusion, and the oxidation of contact plug ingredients, such as polish recon, the contact plug ingredient and the lower electrode material in the interface of a ferroelectric thin film and an electrode, counter diffusion with a ferroelectric thin film, etc., at the elevated temperature in the inside of the oxygen ambient atmosphere for forming a ferroelectric thin film. For this reason, although it is necessary to form thickly the electrode material and barrier metal ingredient which bear an elevated temperature for a long time, the level difference of a capacitor part becomes large by this, and it has been a failure in the case of integrating a component highly. Therefore, in order to make thickness of the whole capacitor thin and to attain high integration, as for a ferroelectric thin film, it is desirable to acquire a good property by low-temperature heat treatment conventionally. As the standard, the heat treatment temperature of a ferroelectric thin film needs to be 650 degrees C or less.

[0020] This invention is made in order to solve the above-mentioned technical problem, it can carry out [low temperature]-izing of the membrane formation temperature compared with the manufacture approach of the conventional ferroelectric thin film, and aims at offering the ferroelectric [which was manufactured by the manufacture approach of a ferroelectric thin film that a manufacture process is simplified, and this manufacture approach] thin film with which it was precise with the ferroelectric and leakage current was reduced, and the ferroelectric memory device which has stack mold structure.

[0021]

[Means for Solving the Problem] In the manufacture approach of the ferroelectric thin film equipped with a lower electrode layer, a ferroelectric thin film, and an up electrode layer in order on a substrate in this invention in order to solve the above-mentioned technical problem The process which applies the precursor solution containing a metal to the front face of said lower electrode layer formed on the substrate, The process which heats the applied precursor solution, removes only a solvent and is dried, It is considering as the manufacture approach of a ferroelectric thin film including the 1st heat treatment process which heats the dried precursor and forms a ferroelectric thin film, and the 2nd heat treatment process heated in a gas pressure ambient atmosphere lower than one atmospheric pressure after forming an up electrode layer on the ferroelectric thin film.

[0022] Furthermore, in this invention, gas pressure of the ambient atmosphere of the 2nd heat treatment process is set to 20 or less Torrs in the manufacture approach of the above-mentioned ferroelectric thin film.

[0023] Furthermore, in this invention, gas pressure of the ambient atmosphere of the 2nd heat treatment process is set to 2 or more-Torr 20 or less Torr in the manufacture approach of the above-mentioned ferroelectric thin film.

[0024] Furthermore, in this invention, heating temperature of the 2nd heat treatment process is made into 500 degrees C or more 650 degrees C or less in the manufacture approach of the above-mentioned ferroelectric thin film.

[0025] Furthermore, in this invention, what uses metaled carboxylate and a metaled alkoxide as a component is used as a precursor solution in the manufacture approach of the above-mentioned ferroelectric thin film.

[0026] Moreover, in this invention, the ferroelectric thin film supposes that the diameter of the maximum crystal grain consists of a bismuth layer structure compound 700A or less in the ferroelectric thin film equipped with the lower electrode layer, the ferroelectric thin film, and the up electrode layer in order on the substrate.

[0027] Moreover, it sets for the semiconductor memory component containing the memory cell equipped with one transistor for a switch, and one ferroelectric capacitor. The semi-conductor substrate top with which the transistor for a switch was formed The insulator thin film of a wrap 1st, The contact plug into which it pierced through the 1st insulator thin film, and the interior was filled up with conductive material,

It has the stack mold structure equipped with the lower electrode formed on the contact plug, the ferroelectric thin film formed on the lower electrode, and the up electrode formed on the ferroelectric thin film, and it is supposed that a ferroelectric thin film consists of a bismuth layer structure compound.
[0028] Furthermore, in this invention, the bismuth layer structure compound which accomplishes a ferroelectric thin film is used as the compound of Ta or Ti which contains either at least in the above-mentioned ferroelectric memory device including Sr and Bi.
[0029] as mentioned above, by the manufacture approach of the ferroelectric thin film of this invention In the manufacture approach of the ferroelectric thin film by the sol gel process or the MOD method After applying to a substrate the precursor solution which consists of the component element of a ferroelectric thin film material and drying, RTA heating down stream processing for carrying out pyrolysis removal of the organic substance component in the conventional film is skipped. A spreading desiccation process is repeated several times and it considers as predetermined thickness, and it crystallizes at the same time the 1st heat treatment process pyrolyzes and removes the organic substance after that. And the ferroelectric thin film is crystallized by performing time amount heating sufficient in a gas pressure ambient atmosphere lower than one atmospheric pressure as the 2nd heat treatment process after forming an up electrode thin film on it. Since the film manufactured by the manufacture approach turns into precise film with small particle diameter by this while low temperature-ization of membrane formation temperature is attained compared with the conventional manufacture approach according to this invention, leakage current is small and that it is [which it is dielectric strength] high can obtain the ferroelectric thin film which was very excellent.
[0030]
[Embodiment of the Invention] Hereafter, the gestalt of the 1st operation by this invention is explained with reference to a drawing. Drawing 1 is the sectional view showing the structure of the ferroelectric thin film by the gestalt of the 1st operation by the manufacture approach of the ferroelectric thin film of this invention. As shown in drawing 1 , this ferroelectric thin film forms the silicon thermal oxidation film 2 of 200nm of thickness in the front face of n mold silicon substrate 1, and sequential formation of the Ta film 3 of 30nm of thickness, the Pt film 4 of 200nm of thickness, 2OSrBi2Ta9 thin film (a SBT thin film is called hereafter) 5 that is a ferroelectric thin film of 200nm of thickness, and the Pt up electrode 6 of 100nm of thickness is carried out on it, respectively. In addition, the silicon thermal oxidation film 2 is formed as an interlayer insulation film, and is not limited to this here. Moreover, since the Pt film 4 forms the oxide film on this, it is chosen as an electrode material which cannot oxidize easily, in addition conductive oxide film, such as RuO2 and IrO2, etc. may be used for it. And the Ta film 3 is used in consideration of the adhesion of the silicon thermal oxidation film 2 and the Pt film 4, in addition Ti film and the TiN film may be used for it.
[0031] Next, the manufacture approach of the ferroelectric thin film shown in drawing 1 is explained.
[0032] First, thickness forms in the front face of n mold silicon substrate 1 the silicon thermal oxidation film 2 which is 200nm. In addition, with the gestalt of this operation, it forms as the formation approach of the silicon thermal oxidation film by oxidizing thermally silicon substrate 1 front face at 1000 degrees C. And on this silicon thermal oxidation film 2, the Ta film 3 whose thickness is 30nm is formed by the spatter, the Pt film 4 whose thickness is 200nm is further formed on this, and this is used as a ferroelectric thin film formation substrate.
[0033] The synthetic approach of the precursor solution hereafter used in order to form the SBT thin film 5 on this substrate, and the process which forms a SBT thin film as a ferroelectric thin film on a substrate using this precursor solution are explained referring to process drawing of drawing 2 .
[0034] As a start raw material of precursor solution composition, tantalum ethoxide (Ta (OC2H5)5), bismuth-2-ethyl hexanate (Bi2 (C7H15COO)), and strontium-2-ethyl hexanate (Sr2 (C7H15COO)) are used. In order to carry out weighing capacity of the tantalum ethoxide (step S1), to make it dissolve into 2-ethyl hexanate (step S2) and to promote a reaction, it agitates heating from 100 degrees C to 120 degrees C of maximum temperatures, and is made to react for 30 minutes (step S3). Then, the ethanol and the moisture which were generated by the reaction at 12 degrees C are removed. Heating churning

of the strontium-2-ethyl hexanate which the 20ml - 30ml xylene was made to dissolve in the solution is carried out for 30 minutes at 140 degrees C of maximum temperatures from optimum dose **** (step S4) and 125 degrees C so that it may be set to Sr/Ta=1/2 (step S5). Then, heating churning of the bismuth-2-ethanol which the 10ml xylene was made to dissolve in this solution is carried out at 150 degrees C of maximum temperatures from optimum dose **** (step S6) and 130 degrees C for 10 hours so that it may be set to Sr/Bi/Ta=1/2.4/2 (step S7).

[0035] Next, in order to remove the xylene used as the alcohol, the water, and the solvent of low molecular weight from this solution, it distills at the temperature of 130 degrees C - 150 degrees C for 5 hours. In order to remove dust from this solution, it **** with the filter of the diameter of 0.45 micrometer (step S8). Then, the concentration of SrBi2.4Ta 2.0O9.6 of a solution is adjusted to 0.1 mol/l, and let this be a precursor solution (step S9). In addition, these raw materials are not limited to the above-mentioned thing, and the above-mentioned start raw material should just dissolve a solvent enough.

[0036] Subsequently, the above-mentioned precursor solution is used and membranes are formed at the following processes. The above-mentioned precursor solution is dropped on a substrate with the lower platinum electrode 4 mentioned above, and spin spreading is carried out by 3000rpm during 20 seconds (step S10). Then, it puts on the hot play which heated the substrate at 120 degrees C, and is made to BEKU and dry in atmospheric air for 5 minutes (step S11). In that case, in order to advance desiccation to homogeneity, it is desirable to make a temperature requirement into 100 degrees C - 130 degrees C, and the optimal drying temperature is about 120 degrees C. Since a crack occurs by membrane stress in the below-mentioned phase which carries out a laminating when it dries at temperature higher than this temperature requirement, for example, 150 degrees C, this is for preventing it.

[0037] Then, in order to volatilize a solvent completely, it puts on the hot plate which heated the wafer at 250 degrees C, and BEKU and calcinates in atmospheric air for 5 minutes (step S12). This temperature is more than the boiling point of a solvent, and it is desirable to carry out at the temperature of 250 degrees C - about 300 degrees C for compaction of process time amount. This membrane formation process is repeated 3 times, and the ferroelectric thin film of 200nm of thickness is formed.

[0038] then — as the 1st baking — RTA — using law, heat treatment for 30 minutes was performed at 600 degrees C among the atmospheric pressure oxygen ambient atmosphere (step S13), and the mask vacuum evaporationo of the Pt up electrode 6 of 200nm of thickness was carried out with EB (electron beam) vacuum deposition (step S14). In this 1st baking, pyrolysis removal of the organic substance contained in the ferroelectric thin film by which spreading desiccation was carried out is performed. And a part of crystallization of a ferroelectric thin film is performed to pyrolysis removal and coincidence of the organic substance, and it is thought that it acts as a kind of nucleation process. in addition -- the gestalt of this operation — RTA — although heat-treated in the atmospheric pressure oxygen ambient atmosphere using law — RTA -- law — the usual heat treating furnace may be used for except, and mixed gas with inert gas, such as oxygen, nitrogen, and an argon, may be used for it as a controlled atmosphere. Moreover, with the gestalt of this operation, as electrode size for ferroelectric characterization, although Pt up electrode was used as the electrode of 100 micrometerphi, this invention is not limited to such electrode configurations or electrode sizes.

[0039] next -- as the 2nd baking (this baking) after up electrode formation — RTA -- baking for 30 minutes is performed at 400 degrees C - 750 degrees C in 10Torr oxygen ambient atmosphere using law (step S15). This 2nd baking is for performing perfect crystallization of a ferroelectric thin film. in addition -- the gestalt of this operation -- RTA -- although calcinated in 10Torr oxygen ambient atmosphere using law -- RTA -- law -- as long as heat treatment is possible for except in a gas pressure ambient atmosphere lower than one atmospheric pressure, the usual heat treating furnace may be used, and as a firing environments, you may be the mixed gas which inert gas, such as nitrogen or an argon, is sufficient as, and was mixed of inert gas, such as nitrogen and an argon, and the oxygen two or more kinds in addition to oxygen. Production of a ferroelectric thin film is completed according to the above process

(step S16).
[0040] Drawing 3 , drawing 4 , and drawing 5 are graphs which show the strong dielectric characteristics to the 2nd burning temperature of the film obtained by the above-mentioned production process. Measurement of strong dielectric characteristics performs applied voltage as 3V to the capacitor of the type shown in drawing 1 using a well-known SOYA tower circuit.
[0041] Drawing 3 is a graph which shows the value of the membranous remanence Pr. Although Pr also decreases with the fall of the 2nd burning temperature, at least 600 degrees C of two or more 4microC/cm values are acquired for the 2nd burning temperature. Drawing 4 is a graph which shows the value of the coercive electric field Ec of the film produced by this manufacture approach, above 500 degrees C, is not based on the 2nd burning temperature, but shows the almost fixed value. Amount of stored charge deltaQ shown in drawing 5 increases like Pr shown in drawing 3 depending on the 2nd burning temperature, and the 2nd burning temperature shows the good property above 500 degrees C.
[0042] Drawing 6 , drawing 7 , and drawing 8 are graphs which show the applied-voltage dependency of the ferroelectric property at the time of performing annealing for 30 minutes in an atmospheric pressure oxygen ambient atmosphere with the 1st burning temperature of 600 degrees C, and performing annealing for 30 minutes for the 2nd baking at 600 degrees C among 10Torr oxygen ambient atmosphere. Respectively drawing 6 , drawing 7 , and drawing 8 show the value of Pr, Ec, and deltaQ, and are a thing, and these graphs show from these that Pr, Ec, and deltaQ are beginning to be saturated from about applied-voltage 3V with the increment in applied voltage. Even if this has change of some electrical potential differences in the applied voltage beyond 3V, it shows that a fixed property is always acquired and can be said to be a good ferroelectric property.
[0043] Drawing 9 is the graph which plotted change of amount of stored charge deltaQ to the count of repeat polarization reversal at the time of impressing electrical-potential-difference 3V and a pulse with a frequency of 1kHz to the sample which performed annealing for 30 minutes in the atmospheric pressure oxygen ambient atmosphere with the 1st burning temperature of 600 degrees C, and performed annealing for 30 minutes for the 2nd baking at 600 degrees C among 10Torr oxygen ambient atmosphere, and performing repeat polarization reversal to it. After polarization reversal of 2x1011 cycle shows a good property to change not being looked at by the amount of stored charge, but completely applying to it at nonvolatile memory.
[0044] Drawing 10 is a graph which shows change of the leakage current over the 2nd burning temperature at the time of 3V impression. Above 550 degrees C, it was not based on the 2nd burning temperature, but had become the value of 6 - 9x10-8 A/cm2, and below 500 degrees C, although leakage current was large, the increment in the leakage current which became a problem conventionally on the occasion of low-temperature-izing of the 2nd burning temperature was not seen.
[0045] Drawing 11 performs annealing for 30 minutes in an atmospheric pressure oxygen ambient atmosphere with the 1st burning temperature of 600 degrees C, and it is the surface SEM photograph of the film after performing annealing for 30 minutes for the 2nd baking at 600 degrees C among 10Torr oxygen ambient atmosphere, and it turns out that it is the precise film which consists of spherical crystal grain 700A or less. Moreover, the 2nd burning temperature became the precise film which consists of spherical crystal grain 700A or less like that whose thing whose 2nd burning temperature is 650 degrees C is also 600 degrees C. On the other hand, annealing was performed for 30 minutes in the atmospheric pressure oxygen ambient atmosphere with the 1st burning temperature of 600 degrees C, and the crystal grain with the still bigger SBT film at the time of performing annealing for 30 minutes at 700 degrees C among the oxygen ambient atmosphere of 10Torr(s) than that whose 2nd burning temperature is 700 degrees C in that whose 2nd burning temperature 500-5000A crystal grain exists by the shape of a string, and is 750 degrees C existed the 2nd baking. The diameter of the maximum crystal grain of the crystal grain child who constitutes the SBT film with the rise of the 2nd burning temperature increased, and the result that the precise film with which the 2nd burning temperature consists of spherical crystal grain 700A or less in 650 degrees C or less could be formed was obtained from these things.

[0046] Although it had become the polycrystal of SrBi2Ta 2O9 with the 2nd burning temperature of 500 degrees C or more as a result of the X diffraction, the clear crystal was not able to be checked below 450 degrees C.

[0047] As an example of a comparison of the gestalt of implementation of the above 1st, the SBT thin film was formed using the conventional manufacture approach, and the ferroelectric thin film which has the same structure as drawing 1 was manufactured for evaluation of the electrical property.

[0048] Drawing 12 is drawing showing the synthetic approach of the precursor solution used in order to form the SBT thin film 5 in the ferroelectric thin film shown in drawing 1 , and the conventional process which forms a SBT thin film as a ferroelectric thin film on a substrate using this precursor solution. The same number is given to the same process as the process of the gestalt of the 1st operation shown in drawing 2 .

[0049] In manufacture of the ferroelectric thin film in this example of a comparison, a different point from the gestalt of the 1st operation of the above-mentioned is only the process of the 2nd baking at the time of formation of a SBT thin film. namely, the SBT film which carried out the mask vacuum evaporationo of the Pt up electrode 6 of 100 micrometerphi after the 1st baking like the gestalt of the 1st operation of the above-mentioned -- receiving -- the thing of the example of a comparison -- as the 2nd baking -- RTA -- 600-750-degree-C baking for 30 minutes was performed in the atmospheric pressure oxygen ambient atmosphere using law (step S20).

[0050] Drawing 13 , drawing 14 , and drawing 15 are graphs which show the strong dielectric characteristics to the 2nd burning temperature of the film obtained at the process of this example of a comparison. Measurement of strong dielectric characteristics performs applied voltage as 3V like the gestalt of implementation of the above 1st to the capacitor of the type shown in drawing 1 using a well-known SOYA tower circuit.

[0051] Drawing 13 is a graph which shows the value of the membranous remanence Pr. When the 2nd burning temperature falls, bordering on 730 degrees C, Pr value decreases rapidly, turns into two or less 2microC/cm and a very small value below 700 degrees C, and are ********** about a ferroelectricity at 600 degrees C. [most] Although two or more 4microC/cm Pr value is acquired with the gestalt of the 1st operation as compared with the gestalt of the above-mentioned's 1st operation of this, the 2nd burning temperature was possible at 600 degrees C, but (refer to drawing 3) in the example of a comparison, if it is not 730 degrees C or more in the 2nd burning temperature, it turns out that two or more 4microC/cm Pr value cannot be acquired. Although equivalent Pr value is acquired from this, it is clear that the gestalt of the 1st operation has realized low temperature-ization of the 2nd burning temperature rather than the thing of the example of a comparison.

[0052] Drawing 14 shows the value of a coercive electric field Ec, above 650 degrees C, is not based on the 2nd burning temperature, but shows the almost fixed value. If amount of stored charge deltaQ shown in drawing 15 becomes the temperature not more than it bordering on the 2nd burning temperature of 730 degrees C like Pr shown in drawing 13 , the value will decrease rapidly.

[0053] Drawing 16 is a graph which shows change of the leakage current over the 2nd burning temperature at the time of 3V impression. Although leakage current increases a single figure at a time and it becomes a fall inclination at 600 degrees C whenever the 2nd burning temperature falls by 50 degrees C, as for a 600-degree C thing, a ferroelectricity is hardly shown.

[0054] After drawing 17 performs annealing for 30 minutes in an atmospheric pressure oxygen ambient atmosphere with the 1st burning temperature of 600 degrees C and performs annealing for 30 minutes for the 2nd baking at 700 degrees C among an atmospheric pressure oxygen ambient atmosphere, it is the surface SEM photograph of the film of **. As for the SBT film in this case, existence of 1500-9000A crystal grain exists by the shape of a string.

[0055] Here, it compares with the thing of the gestalt of the 1st operation of the above-mentioned, and the thing of this example of a comparison about the size of crystal grain. Although crystal grain was 500-5000A by the SBT film at the time of performing annealing for 30 minutes in an atmospheric pressure oxygen ambient atmosphere with the 1st burning temperature of 600 degrees C, and

performing annealing for 30 minutes for the 2nd baking at 700 degrees C among the oxygen ambient atmosphere of 10Torr(s) as above-mentioned, in this example of a comparison, it is 1500-9000A as above-mentioned, and the way of the thing of the gestalt of the 1st operation serves as small crystal grain from the thing of the example of a comparison. According to the comparison of these SBT film formed only on condition that the ambient-gas-pressure force of the 2nd baking differing from this in the film in which a ferroelectricity is shown, it is clear by performing the 2nd baking in a gas pressure ambient atmosphere lower than one atmospheric pressure for membranous eburnation to be possible.

[0056] Subsequently, it compares with the thing of the gestalt of the 1st operation of the above-mentioned about the size of the crystal grain of a ferroelectric thin film and the thing of this example of a comparison from which a remanence Pr value becomes almost equivalent. In the gestalt of the 1st operation of the above-mentioned, as annealing is performed for 30 minutes in an atmospheric pressure oxygen ambient atmosphere with the 1st burning temperature of 600 degrees C and the SBT film at the time of performing annealing for 30 minutes at 600 degrees C among the oxygen ambient atmosphere of 10Torr(s) showed the 2nd baking to drawing 3 , Pr value was about 4.2microC/cm2, and crystal grain was 700A or less. On the other hand, as that from which Pr value becomes almost equivalent to this in the example of a comparison, it was Pr value =about 4.3microC/cm2 which performed annealing for 30 minutes in the atmospheric pressure oxygen ambient atmosphere with the 1st burning temperature of 600 degrees C, and performed annealing for 30 minutes for the 2nd baking at 730 degrees C among the atmospheric pressure oxygen ambient atmosphere (refer to drawing 13), and as a result of observing this SBT film front face, the magnitude of that crystal grain was 1500-9000A. If these are compared, the way of the thing of the gestalt of the 1st operation serves as crystal grain smaller than the thing of the example of a comparison. Also in the comparison of the SBT film with which almost equivalent Pr value is acquired from this, it is clear by performing the 2nd baking in a gas pressure ambient atmosphere lower than one atmospheric pressure for membranous eburnation to be possible.

[0057] Although it had become the polycrystal of SrBi2Ta 2O9 with the 2nd burning temperature of 650 degrees C or more in the example of a comparison as a result of the X diffraction, clear crystallization was not able to be checked below 600 degrees C.

[0058] As mentioned above, although 730 degrees C or more needed to be calcinated by the conventional manufacture approach to see increase of a rapid reduction of Pr and delta Q value, and leakage current, and use it as ferroelectric random-access memory when the 2nd burning temperature was lowered According to the gestalt of the 1st operation, while suppressing a rapid reduction of Pr accompanying the fall of the 2nd burning temperature, and delta Q value by [which are depended on this invention] performing the 2nd baking in a gas pressure ambient atmosphere lower than one atmospheric pressure, the increment in leakage current can also be controlled. Thereby, property sufficient as ferroelectric memory with the highest burning temperature of 650 degrees C or less is acquired, and it becomes possible to adopt stack structure required for high integration of FRAM. Moreover, it is suitable also for micro processing and suitable for manufacture of a high density device while the manufacture approach of the gestalt this operation controls a crystal grain child's big and rough-ization, and can realize membranous eburnation and surface flattening and the proposal of leakage current of it is attained.

[0059] Hereafter, the gestalt of the 2nd operation by this invention is explained, referring to a drawing. Drawing 18 is the important section sectional view of the ferroelectric memory cell by this invention which is the gestalt of the 2nd operation. As shown in drawing 18 , the ferroelectric memory cell of the gestalt of this operation On the 1st conductivity-type silicon substrate 54, the components separation oxide film 39 and gate oxide 40, The 2nd conductivity-type impurity diffusion field 41 and polish recon word line 42, It has interlayer insulation films 43, 44, 51, and 52, the memory section contact plug 45, the TiN barrier metal layer 46, the Pt lower electrode 47, the ferroelectric thin film 48, Pt plate line 49, the Ta2O5 barrier insulator layer 50, and the aluminum bit line 53.

[0060] Next, the manufacture approach of this ferroelectric memory cell is explained using drawing 19 which is the explanatory view showing the example of the manufacture approach of the ferroelectric

random-access memory of the structure shown in drawing 18 .
[0061] a phot only with the part well-known as shown in drawing 19 (a), after forming the transistor for a switch with a well-known MOSFET formation process and covering with an interlayer insulation film 43 to which a bit line contacts the impurity diffusion field 41 of a substrate -- well-known CMP (Chemical Mechanical Polishing) after embedding the polish recon which dug and carried out impurity diffusion of the contact hole using the lithography method and the dry etching method -- flattening of the front face of the polish recon plug 45 is carried out to an interlayer insulation film 43 by law.
[0062] Next, as shown in drawing 19 (b), after depositing the TiN barrier metal layer 46 2000A of thickness by the well-known spatter, the Pt thin film 47 is deposited 1000A of thickness by the well-known spatter, and it considers as a lower electrode. Although 2OSrBi2Ta9 thin film (a SBT thin film is called hereafter) is formed as a ferroelectric thin film 48 on this lower electrode The synthetic approach of the precursor solution used in order to form a SBT thin film, and among the processes which form a SBT thin film using this precursor solution, the process to the 1st baking Since it is the same as the process from step S1 of drawing 2 explained with the gestalt of the 1st operation of the above-mentioned to step S13, explanation is omitted.
[0063] It considers as a configuration as processes the magnitude of 3.0-micrometer angle and shows the SBT film 48 after the 1st baking, the Pt lower electrode 47, and the TiN barrier metal layer 46 to drawing 19 (b) using the well-known phot lithography method and the dry etching method. For the SBT film, the mixed gas of Ar, and Cl2 and CF4 and Pt lower electrode are [the mixed gas of C2F6, and CHF3 and Cl2 and the TiN barrier metal of the type of gas used for dry etching using the ECR etcher] Cl2 gas. Since the SBT film and Pt lower electrode are very precise and it is flat at this time, precise micro processing is possible and a CD loss can be held down to 0.1 micrometers or less.
[0064] Next, as shown in drawing 19 (c), the Ta2O5 barrier insulator layer 50 of 300A of thickness is deposited using a well-known spatter, then silicon oxide of 1500A of thickness is deposited with a well-known CVD method as an interlayer insulation film 51, and the contact hole of 2.0-micrometer angle is formed in the SBT film upper part after that using the well-known phot lithography method and the dry etching method.
[0065] next, it is shown in drawing 19 (d) -- as -- Pt up electrode of 1000A of thickness -- a well-known spatter -- forming -- a well-known phot -- as the 2nd heat treatment after processing it using the lithography method and the dry etching method and considering as the plate line 49 -- RTA -- heat treatment for 30 minutes was performed at 600 degrees C in the oxygen ambient atmosphere of 10Torr(s) using law, and the SBT film was crystallized. The cross section of the SBT film after making it crystallize is very smooth too, is precise, and did not spoil the configuration of a ferroelectric capacitor. Moreover, it was 2000A when the thickness of the SBT film was measured.
[0066] Then, an interlayer insulation film 52 is deposited using a CVD method with a well-known flattening technique, flattening is performed, the contact hole to another impurity diffusion field of the transistor for a switch is formed using the well-known phot lithography method and the dry etching method, a bit line 53 is formed using well-known aluminum wiring technique, and a ferroelectric memory cell as shown in drawing 18 is completed.
[0067] Thus, the electrical property of the manufactured ferroelectric memory cell was measured using the well-known SOYA tower circuit. Drawing 20 is a graph which shows the hysteresis loop when measuring applied voltage by 3V. The configuration of the hysteresis loop is good, as for Remanence Pr, 5microC/cm2 is obtained, as for the coercive electric field Ec, the value of 30 kV/cm (0.6V) is acquired, and actuation sufficient as a ferroelectric capacitor was checked. Moreover, by applied-voltage 3V, the value of leakage current is 5x10-8 A/cm2, and property sufficient as a ferroelectric capacitor was checked.
[0068] Drawing 21 is the graph which impressed electrical-potential-difference 3V and a pulse with a frequency of 1MHz, and plotted change of amount of stored charge deltaQ to the count of repeat polarization reversal at the time of performing polarization reversal repeatedly. Change is not looked at by the amount of stored charge, but after polarization reversal of 2x1011 cycle completely shows a

property good as nonvolatile memory to it.
[0069] Hereafter, the gestalt of the 3rd operation by this invention is explained, referring to a drawing. The gestalt of the 3rd operation explains the relation of the crystal grain child's diameter of the maximum crystal grain and the amount of stored charge which constitute the SBT film about the same ferroelectric thin film as the gestalt of the 1st operation of the above-mentioned.
[0070] The point that the ferroelectric thin film of the gestalt of the 3rd operation differs from the gestalt of the 1st operation of the above-mentioned is only a point of having divided the configuration of the Pt up electrode 6 of drawing 1 into the plurality of 2-micrometer angle, and structure, the manufacture approach of it, etc. are completely the same as that of the gestalt of the 1st operation as well as the formation process of the SBT film except it.
[0071] Drawing 22 shows the variation in amount of stored charge deltaQ to the diameter of the maximum crystal grain of the SBT film when measuring by 100 places of Pt up electrode of 2-micrometer angle about the ferroelectric thin film of the capacitor structure of the gestalt of the 3rd operation. In drawing 22 , an axis of ordinate shows the value which broke the standard deviation (sigma) of amount of stored charge deltaQ by the average (deltaQAVE) of amount of stored charge deltaQ, and an axis of abscissa shows the diameter of the maximum crystal grain of the SBT film. According to drawing 22 , with the film with the diameter of the maximum crystal grain smaller than 1000A, dispersion in amount of stored charge deltaQ has very small sigma/delta QAVE at 10% or less, and the diameter of the maximum crystal grain shows that the property that a sigma/delta QAVE value is large and stable is hard to be acquired by the film 1000A or more. Therefore, as the gestalt of the 1st operation of the above-mentioned explained, in the case where the 2nd burning temperature is 650 degrees C or less, it turns out that the diameter of the maximum crystal grain is the good thing which does not almost have dispersion in strong dielectric characteristics at this time since the precise film 700A or less is obtained. In order to have sufficient amount of stored charge for using as a dielectric capacitor and to obtain the SBT film with little dispersion in a property from this, as for the 2nd burning temperature, it is desirable that it is the range of 500 degrees C - 650 degrees C.
[0072] Hereafter, the gestalt of the 4th operation by this invention is explained, referring to a drawing. step S15 of drawing 2 of the gestalt of the 1st operation of the above-mentioned with the gestalt of the 4th operation — setting — as the 2nd baking (this baking) — RTA — baking for 30 minutes is performed at 600 degrees C in a 1 - 760Torr oxygen ambient atmosphere using law, and the production process of component structure and others etc. is completely the same as that of the gestalt of the 1st operation except it. In addition, since the SBT film formed at the time of 1Torr hardly showed a ferroelectricity, having set the range of the ambient-gas-pressure force (the 2nd baking pressure) of the 2nd baking to 1 - 760Torr makes this a minimum, and it makes an upper limit 760Torr(s) which are atmospheric pressure here.
[0073] Drawing 23 , drawing 24 , and drawing 25 are graphs which show the strong dielectric characteristics to the ambient-gas-pressure force (the 2nd baking pressure) of the 2nd baking of the film obtained by the above-mentioned production process. Measurement of strong dielectric characteristics performs applied voltage as 3V to the capacitor of the type shown in drawing 1 using a well-known SOYA tower circuit.
[0074] Drawing 23 is a graph which shows the value of the remanence Pr of the film to the ambient-gas-pressure force (the 2nd baking pressure) of the 2nd baking. Although the ambient-gas-pressure force hardly showed a ferroelectricity by 760Torr(s), if gas pressure falls, Pr value will increase and will serve as the maximum near pressure 5Torr, and if a pressure declines further from it, Pt value will decrease. As for the remanence Pr at the time of pressure 5Torr, property with 5.5microC/cm2 and a coercive electric field Ec sufficient as 25 kV/cm and a ferroelectric capacitor was acquired. Moreover, from drawing 23 , if the ambient-gas-pressure force (the 2nd baking pressure) of the 2nd baking is the range of 2Torr(s) - 20Torr, Pr becomes two or more 2.5microC/cm, and shows sufficient strong dielectric characteristics.
[0075] Drawing 24 is a graph which shows the value of membranous amount of stored charge deltaQ to

the ambient-gas-pressure force (the 2nd baking pressure) of the 2nd baking. A value will increase, amount of stored charge deltaQ as well as Remanence Pr will become the maximum near pressure 5Torr, if the ambient-gas-pressure force declines from 760Torr(s), and if a pressure declines further from it, a value will decrease. The outstanding value of 10.2microC/cm2 in amount of stored charge deltaQ at the time of pressure 5Torr was acquired. Moreover, if it is generally the ferroelectric random-access memory of the degree of integration of an Mbit class, the two or more 5microC/cm amount of stored charge is required. Therefore, if amount of stored charge deltaQ is two or more 5microC/cm in the range of 2Torr(s) - 20Torr and the ambient-gas-pressure force (the 2nd baking pressure) of the 2nd baking is manufactured with the pressure of this range, amount of stored charge deltaQ required as ferroelectric random-access memory of the degree of integration of an Mbit class can be obtained from drawing 24 . Furthermore, as a result of observing the SBT film manufactured by this 2nd baking pressure, it can be checking that it is precise and surface surface smoothness is also good.

[0076] Drawing 25 is a graph which shows the value of the membranous coercive electric field Ec to the ambient-gas-pressure force (the 2nd baking pressure) of the 2nd baking. in the range of 2Torr(s) - 200Torr, the 2nd baking pressure is about 1 law near 25 kV/cm.

[0077] Drawing 26 is a graph which shows change of the leakage current when impressing 3V to the ambient-gas-pressure force (the 2nd baking pressure) of the 2nd baking. Also in which gas pressure, the good value of 10-7 to ten to eight sets is acquired for the 2nd baking pressure.

[0078] Drawing 27 is drawing showing the X diffraction pattern of the film to the ambient-gas-pressure force (the 2nd baking pressure) of the 2nd baking. In drawing 27 , the 2nd baking pressure of a, b, c, d, e, and f is the thing of 760Torr(s), 200Torr, 20Torr, 10Torr, 2Torr, and 1Torr, respectively. Moreover, in drawing 27 , although an axis of abscissa is angle-of-diffraction whenever 2theta (deg) and an axis of ordinate is diffraction reinforcement (arbitration reinforcement), with the axis of ordinate, the location which serves as the diffraction reinforcement 0 about each 2nd baking pressure is moved. And the diffraction peak according [the diffraction peak according / SBT (008), SBT (105), SBT (110), and SBT (200) / to SrBi2Ta 2O9 (SBT), delta-TaO (001) and delta-TaO (001)] to the delta phase TaO, the diffraction peak according [Si] to a silicon substrate, and Pt express the diffraction peak by Pt lower electrode among drawing 27 .

[0079] According to drawing 27 , the polycrystal peak (SBT (008), SBT (105), SBT (110), SBT (200)) of SBT has appeared, in the thing of 1Torr, there is no SBT peak and the peak (delta-TaO (001), delta-TaO (002)) of TaO has appeared at the thing of 2Torr - 200Torr. and by the thing of 760Torr, the SBT peak is broadcloth very much and it is thought that it is the amorphous -like film. According to the observation result of this X diffraction, it turns out that the film in which a SBT peak is shown was obtained in the range of 2Torr - 200Torr as ambient-gas-pressure force of the 2nd baking.

[0080] Drawing 28 is a graph which shows change of the film presentation ratio to the ambient-gas-pressure force (the 2nd baking pressure) of the 2nd baking. since Ta presentation and Sr presentation were not dependent on the 2nd baking pressure and Bi presentation changed to having been about 1 law depending on the 2nd baking pressure as a result of [which depends a SBT film presentation on EPMA] measuring, drawing 28 graph-izes the presentation ratio of Bi/Ta and Sr/Ta. According to drawing 28 , by 760Torr, the value of Bi/Ta is almost the same as the presentation ratio (Bi/Ta=2.4 / 2= 1.2) of a raw material charge, and 2Torr decreases gently with the fall of the 2nd baking pressure, and it serves as stoichiometry (Bi/Ta=1.0) near the 5Torr.

[0081] And by 1Torr, the value of Bi/Ta is [the 2nd baking pressure] small rapidly. It is thought that change of such a Bi presentation originates in the volatilization of Bi or the diffusion to an electrode having taken place at the time of the 2nd baking, and it is thought that it is the cause by which a big gap of such a Bi presentation is the thing of 2nd baking pressure 1Torr, and a ferroelectricity was hardly acquired. On the other hand, since Ta presentation and Sr presentation were not dependent on the 2nd baking pressure and were almost fixed as above-mentioned, Sr/Ta was also almost fixed and almost the same as the presentation ratio (Sr/Ta=1 / 2= 0.5) of a raw material charge.

[0082] In addition, in the above-mentioned gestalt of the 1st - the 4th operation, although SBT (SrBi2Ta

2O9) was used as an ingredient of a ferroelectric thin film An ingredient is not limited to this and besides SrBi2(Ti, Nb)2O9 which are the compound of Ta or Ti which contains either at least, SrBi4Ti 4O15, ** with desirable SrBi4(Ti, Zr)4O15, and these including Sr and Bi SrBi2 </SUB> This invention is applicable if it is the bismuth layer structure compound ingredient which can form membranes by a sol gel process or the MOD methods, such as Nb 2O9, Bi4Ti 3O12, CaBi2Ta 2O9, BaBi2Ta 2O9, BaBi2Nb 2O9, and PbBi2Ta 2O9.

[0083]

[Effect of the Invention] In the manufacture approach of the ferroelectric thin film [according to the manufacture approach of the ferroelectric thin film of this invention] by the sol gel process or the MOD method After applying the precursor solution which consists of the component element of a ferroelectric thin film material and drying, the heat-treatment for carrying out pyrolysis removal of the organic substance component in the film is omitted. By heating in a gas pressure ambient atmosphere lower than one atmospheric pressure as the 2nd heat treatment process, after repeating a spreading desiccation process several times, considering as predetermined thickness and forming a ferroelectric thin film according to the 1st heat treatment process after that The ferroelectric thin film is crystallized and low temperature-ization of membrane formation temperature is attained from the conventional approach. Furthermore, the film produced by the manufacture approach of the ferroelectric thin film of this invention turns into precise film with small particle diameter, and leakage current can obtain the small high ferroelectric thin film of dielectric strength.

[0084] More, in order for the conventional manufacture approach to set, to hardly crystallize upwards in the burning temperature of 650 degrees C or less and to acquire a property required as ferroelectric random-access memory, 730 degrees C or more needed to be calcinated for the detail, but since low temperature-ization of 100 degrees C or more is attained from the conventional manufacture approach by the manufacture approach of this invention and property sufficient as memory also with the burning temperature of the low temperature of 600 degrees C is acquired, integration using the stack structure of ferroelectric random-access memory is attained.

[0085] Moreover, since the thin film produced by the manufacture approach of the ferroelectric thin film of this invention controls a crystal grain child's big and rough-ization, can realize membranous eburnation and surface flattening and also fits micro processing, manufacture of a higher-density device is realizable.

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the sectional view of the gestalt of operation of the 1st of the ferroelectric thin film by this invention.
[Drawing 2] It is process drawing showing a part of production process of the ferroelectric thin film of drawing 1 .
[Drawing 3] It is the graph which shows change of the remanence Pr over the 2nd burning temperature of the ferroelectric thin film of drawing 1 .
[Drawing 4] It is the graph which shows change of the coercive electric field Ec to the 2nd burning temperature of the ferroelectric thin film of drawing 1 .
[Drawing 5] It is the graph which shows change of amount of stored charge deltaQ to the 2nd burning temperature of the ferroelectric thin film of drawing 1 .
[Drawing 6] It is the graph which shows change of the remanence Pr over the applied voltage of the ferroelectric thin film of drawing 1 .
[Drawing 7] It is the graph which shows change of the coercive electric field Ec to the applied voltage of the ferroelectric thin film of drawing 1 .
[Drawing 8] It is the graph which shows change of amount of stored charge deltaQ to the applied voltage of the ferroelectric thin film of drawing 1 .
[Drawing 9] It is drawing showing the fatigue property of the ferroelectric thin film of drawing 1 .
[Drawing 10] It is the graph which shows change of the leakage current at the time of 3V impression to the 2nd burning temperature of the ferroelectric thin film of drawing 1 .
[Drawing 11] It is the SEM photograph of the membranous front face which manufactured 600 degrees C and the 2nd burning temperature for the 1st burning temperature as 600 degrees C by the manufacture approach of drawing 2 .
[Drawing 12] It is drawing showing a part of production process of the conventional ferroelectric thin film.
[Drawing 13] It is the graph which shows change of amount of stored charge deltaQ to the 2nd burning temperature of the conventional ferroelectric thin film.
[Drawing 14] It is the graph which shows change of the coercive electric field Ec to the 2nd burning temperature of the conventional ferroelectric thin film.
[Drawing 15] It is the graph which shows change of the coercive electric field Ec to the 2nd burning temperature of the conventional ferroelectric thin film.
[Drawing 16] It is the graph which shows change of the leakage current at the time of 3V impression to the 2nd burning temperature of the conventional ferroelectric thin film.
[Drawing 17] It is the SEM photograph of the membranous front face which manufactured 600 degrees C and the 2nd burning temperature for the 1st burning temperature as 600 degrees C by the conventional manufacture approach.
[Drawing 18] It is the sectional view of the ferroelectric random-access memory of the gestalt of the 2nd operation by this invention.
[Drawing 19] It is the sectional view showing a part of production process of the ferroelectric random-

access memory of drawing 18 .

[Drawing 20] It is the graph which shows the hysteresis loop when impressing the electrical potential difference of 3V to the SBT ferroelectric random-access memory of drawing 18 .

[Drawing 21] It is the graph which shows the fatigue property of the SBT ferroelectric random-access memory of drawing 18 .

[Drawing 22] It is the graph which shows the value change which broke the standard deviation (sigma) of amount of stored charge deltaQ to the diameter of the maximum crystal grain of the ferroelectric thin film of the ferroelectric thin film of the gestalt of the 3rd operation by this invention by the average (deltaQAVE) of amount of stored charge deltaQ.

[Drawing 23] It is the graph which shows change of the remanence Pr of the film to the ambient-gas-pressure force (the 2nd baking pressure) of the 2nd baking of the ferroelectric thin film of the gestalt of the 4th operation by this invention.

[Drawing 24] It is the graph which shows change of amount of stored charge deltaQ to the ambient-gas-pressure force (the 2nd baking pressure) of the 2nd baking of the ferroelectric thin film of the gestalt of the 4th operation.

[Drawing 25] It is the graph which shows change of the coercive electric field Ec to the ambient-gas-pressure force (the 2nd baking pressure) of the 2nd baking of the ferroelectric thin film of the gestalt of the 4th operation.

[Drawing 26] It is the graph which shows change of the leakage current at the time of 3V impression to the ambient-gas-pressure force (the 2nd baking pressure) of the 2nd baking of the ferroelectric thin film of the gestalt of the 4th operation.

[Drawing 27] It is drawing showing the X diffraction pattern of the film to the ambient-gas-pressure force (the 2nd baking pressure) of the 2nd baking of the SBT film of the ferroelectric thin film of the gestalt of the 4th operation.

[Drawing 28] It is the graph which shows change of the film presentation ratio to the ambient-gas-pressure force (the 2nd baking pressure) of the 2nd baking of the SBT film of the ferroelectric thin film of the gestalt of the 4th operation.

[Description of Notations]

1 Si Substrate
2 SiO2
4 Lower Electrode Layer
5 48 Ferroelectric thin film
6 Up Electrode Layer
41 2nd Conductivity-Type Impurity Diffusion Field
43, 44, 51, 52 Interlayer insulation film
45 Memory Section Contact Plug
47 Lower Electrode
49 Plate Line
54 1st Conductivity-Type Silicon Substrate

[Translation done.]